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54 Programmable read only memory.

57 Unique EPROM and EEPROM devices are provided with a composite dielectric layer between the control gate and the floating gate which is sufficiently thick to provide electrical and physical integrity but also has a high equivalent dielectric constant. The use of the composite dielectric layer alleviates certain problems experienced in the prior art EPROM and EEPROM devices which utilize a polycrystalline silicon floating gate and a polycrystalline silicon control gate separated by an SiO<sub>2</sub> dielectric layer, such as the problems of sharp silicon points polysilicon grain growth causing low dielectric breakdown strength. In contrast to the prior art, a composite dielectric layer serves as a partially relaxable dielectric between the control gate and the floating gate of an EEPROM or an EPROM. The composite dielectric layer provides high capacitance between the floating gate and the control gate without the insulative and breakdown problems encountered with prior art thin dielectric layers, with electron injection taking place through the gate oxide between the drain extension and the floating gate, (EEPROM), and between the channel and the floating gate (EPROM). In another embodiment of this invention, the composite dielectric layer is implemented between the drain extension (EEPROM) or the channel (EPROM) and the floating gate and serves as the tunnel oxide.

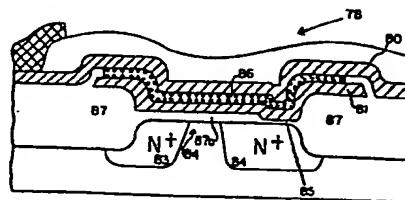


FIG. 6

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1                   PROGRAMMABLE READ ONLY MEMORY

2  
3  
4                   BACKGROUND OF THE INVENTION

5  
6                   Field of the Invention

7  
8                   This invention relates to a Programmable Read Only  
9                   Memory structure and more particularly to a novel  
10                  integrated circuit structure for the cells of such a  
11                  memory.

12  
13  
14  
15                  Description of the Prior Art

16  
17                  Integrated circuit memory devices are known in the  
18                  prior art. Figure 1a shows a cross-sectional view of a  
19                  typical Metal Oxide Silicon (MOS) Electrically Erasable  
20                  Programmable Read Only Memory (EEPROM) cell 19 capable of  
21                  storing a single binary digit ("bit"). Cell 19 includes P  
22                  type substrate 10, N type drain 11b, N type source 11a,  
23                  channel region 13, floating gate 15, control gate 16,  
24                  tunnel oxide 12 between floating gate 15 and drain extension  
25                  11c, dielectric oxide 18 located between floating gate 15  
26                  and control gate 16, field oxide 17, and electrical contacts  
27                  14a and 14b. Floating gate 15 is capacitively coupled to  
28                  control gate 16 through dielectric oxide 18.

29  
30                  To program cell 19 to store a logical "one", the  
31                  drain 11b is connected to a high voltage (typically  
32                  approximately 21 volts) through contact 14b, and source  
33                  11a is either connected to a small positive voltage  
34                  (approximately 3 volts) through contact 14a or left  
35                  unconnected ("floating"). Control gate 16 is connected to  
36                  ground. The ground voltage on control gate 16 is capaci-  
37                  tively coupled to floating gate 15, thereby holding floating  
38

1 gate 15 near ground potential. Because of the high positive  
2 voltage placed on drain 11b and drain extension 11c,  
3 electrons in the floating gate 15 tunnel through the  
4 tunnel oxide 12 into the drain extension 11c, thus leaving  
5 a net positive charge on floating gate 15. When program-  
6 ming is complete, floating gate 15 retains this positive  
7 charge, thus decreasing the voltage required to be placed  
8 on control gate 16 to render cell 19 conductive. Thus  
9 cell 19, having a decreased control gate threshold voltage  
10 (i.e. the voltage on control gate 16 required to turn cell  
11 19 on), stores a logical one. The control gate threshold  
12 voltage for a cell 19 which has been programmed to store a  
13 logical one is typically zero or slightly negative (e.g.  
14 -3 volts). A cell 19 which is not programmed by placing a  
15 positive charge on floating gate 15 has a typical control  
16 gate threshold voltage of 1 volt.

17  
18 To erase cell 19, ground voltage is applied to drain  
19 11b via contact 14b and a high positive erase voltage  
20 (typically approximately 20 volts) is applied to control  
21 gate 16. Electrons then flow from drain extension 11c  
22 through tunnel oxide 12 to floating gate 15 thereby  
23 discharging floating gate 15 to zero or to a slightly  
24 negative voltage. To turn on erased cell 19, a rather  
25 high positive voltage on the control gate 16 is needed and  
26 the control gate threshold voltage for an "erased" cell 19  
27 is, for example, approximately +5 volts.

28  
29 To read cell 19, drain 11b is connected to a small  
30 positive voltage (typically approximately 2 volts) and  
31 source 11a is grounded. A sense amplifier (not shown)  
32 detects the current flowing through drain 11b. A read  
33 voltage (typically approximately 2 volts) is placed on  
34 control gate 16 which is sufficiently positive to turn on  
35 cell 19 when cell 19 stores a logical one (i.e. floating  
36 gate 15 is charged positive), but which is not sufficiently  
37 positive to turn on cell 19 when cell 19 stores a logical  
38

1 zero (i.e. floating gate 15 is charged to zero or slightly  
2 negative). The sense amplifier senses the drain current  
3 of cell 19, which in turn indicates if cell 19 is turned  
4 on or off, which is determined by the logical state (i.e.  
5 logical one or zero) of the bit stored in cell 19. Thus,  
6 the data stored in cell 19 is read.

7  
8 An array of EEPROM cells forming an EEPROM device can  
9 be made with supporting periphery circuitry which allows  
10 selective programming, erasing and reading. Such an array  
11 is described, for example in "A 16Kb Electrically Erasable  
12 Nonvolatile Memory" by W. S. Johnson et al., 1980 IEEE  
13 International Solid-State Circuits Conference, P. 152,  
14 1980.

15  
16 Figure 1b shows a typical prior art Erasable Program-  
17 mable Read Only Memory (EPROM) cell 24, containing a  
18 control gate 25, floating gate 26, N type source region  
19 28a, N type drain region 28b, dielectric 27, field oxide  
20 29, gate oxide 30, P type channel 32 and P type substrate  
21 31. To program cell 24, high positive voltages (typically  
22 approximately 20 volts) are applied to drain 28b and  
23 control gate 25, and source 28a is grounded. The high  
24 voltage applied to control gate 25 is capacitively coupled  
25 to the floating gate 26, which causes channel 32 to conduct,  
26 thus turning cell 24 on. Because of the high drain voltage,  
27 a rather large quantity of "hot" electrons are generated  
28 in the channel 32, such "hot" electrons having sufficiently  
29 high energy to overcome the potential barrier of gate  
30 oxide 30. These hot electrons are attracted to and collected  
31 by the floating gate 26, which is at a positive potential  
32 due to the positive voltage applied to control gate 25.  
33 These hot electrons which are collected on the floating  
34 gate 26 make the floating gate voltage negative and thus  
35 raise the control gate threshold voltage of cell 24 by  
36 several volts--and a logical "one" bit is stored in cell  
37 24. To read cell 24, read voltages (typically 2 to 3  
38

1 volts) are applied to drain 28b and control gate 25, and  
2 source 28a is grounded. The read voltage applied to  
3 control gate 25 is such that it is not sufficiently high  
4 to turn on cell 24 when cell 24 stores a logical one, but  
5 is sufficiently high to turn on cell 24 when cell 24  
6 stores a logical zero. A sense amplifier (not shown) is  
7 used in a similar fashion as previously described in  
8 conjunction with the EEPROM of Figure 1a, to sense the  
9 data stored in cell 24.

10

11 To erase EPROM cell 24, UV (ultra-violet) light is  
12 used to illuminate the floating gate 26. The passivation  
13 oxide 27 surrounding the floating gate is transparent to  
14 UV light. UV light has sufficiently high photon energy to  
15 impart sufficient energy to the electrons on the floating  
16 gate 26 to cause the electrons to overcome the barrier of  
17 oxide 30 and leak out from the floating gate 26 to channel  
18 32, thereby discharging floating gate 26.

19

20 An array of EPROM cells forming an EPROM device can  
21 be made with supporting periphery circuitry which allows  
22 selective programming and reading. Erase is done for  
23 entire array with UV light illumination. Such an array of  
24 EPROM cells is described, for example, by G. Perlegos et  
25 al., in "A 64K EPROM using Scaled MOS Technology", 1980  
26 IEEE International Solid-State Circuits Conference, Page  
27 142, 1980.

28

29 In integrated circuit capacitors and more particu-  
30 larly in memory devices, a thin dielectric layer between  
31 two conductive layers capacitively couples the conductive  
32 layers. For example, in Erasable Programmable Read Only  
33 Memory (EPROM) memory cells (Fig. 1b) or Electrically  
34 Erasable Programmable Read Only Memory (EEPROM) cells  
35 (Figure 1a), a floating gate (for example floating gate 15  
36 of Figure 1a) is typically separated from the control gate  
37 16 (Figure 1a) by a thin dielectric layer 18 of silicon

38

1 dioxide ( $\text{SiO}_2$ ), or Silicon Nitride ( $\text{Si}_3\text{N}_4$ ). It is essential  
2 that this dielectric layer is very thin in order that the  
3 capacitance between the control gate 16 and floating gate  
4 15 is large compared with the capacitance between the  
5 floating gate 15 and other regions (e.g., between floating  
6 gate 15 and drain extension 11c), thereby causing the  
7 voltage on floating gate 15 to closely follow the voltage  
8 on control gate 16, thus allowing a large voltage drop  
9 across the tunnel oxide 12 to induce tunneling current  
10 during programming and erasing. However, the thin layer  
11 of dielectric 18 must be of excellent insulative quality  
12 so that the charge stored on the floating gate 15 does not  
13 leak out over extended periods of time (i.e. 10 yrs at  
14  $125^\circ\text{C}$ ), thereby discharging floating gate 15. Providing a  
15 dielectric layer which is both very thin and of excellent  
16 insulative quality is very difficult. For instance, when  
17 the dielectric layer 18 is made excessively thin (i.e. 500  
18 angstroms or less) high capacitance between floating gate  
19 15 and control gate 16 is achieved, but the dielectric  
20 integrity and insulation properties of dielectric layer 18  
21 are poor. Thus, if a defect exists in dielectric layer  
22 18, control gate 16 may become electrically connected to  
23 floating gate 15, thus causing an electrical failure of  
24 the device. Alternatively, the poor insulative quality of  
25 dielectric 18 allows undesirable charging or discharging  
26 of floating gate 15 via control gate 16. In order to  
27 prevent such defects in dielectric layer 18, dielectric  
28 layer 18 must be formed to a minimum thickness of about  
29 600-700Å when  $\text{SiO}_2$  is used as dielectric 18. The use of  
30 this rather thick oxide as dielectric 18 requires a large  
31 overlap area between control gate 16 and floating gate 15  
32 in order to achieve the necessary capacitance between  
33 floating gate 15 and control gate 16. This large overlap  
34 area causes the cell size to be rather large. Large cell  
35 size, and thus large device size, is very undesirable in  
36 that the product yield rate decreases drastically with an  
37 increase in chip size.  
38

1 Typically, control gate 16 and floating gate 15 are  
2 formed of doped polycrystalline silicon (often called  
3 "polysilicon" or "poly" for short) because of the well-  
4 known advantages of polysilicon gate technology. At  
5 least two problems exist with the use of a "sandwich"  
6 formed of polysilicon floating gate 15,  $\text{SiO}_2$  dielectric  
7 18, and polysilicon control gate 16. One such problem is  
8 the asperities (as shown in Figure 2) which are rough  
9 points at the polysilicon/ $\text{SiO}_2$  interfaces between control  
10 gate 16 and dielectric 18, and between dielectric 18 and  
11 floating gate 15. As shown in Figure 2, the presence of  
12 sharp points C formed by the uneven distribution of silicon  
13 atoms along interfaces A and B cause local high electric  
14 fields at points C and thus dielectric breakdown problems  
15 at sharp points C, even with a relatively low voltage  
16 difference between control gate 16 and floating gate 15.  
17 The low voltage breakdown at point C may occur at 3 to 4  
18 times lower voltage compared to a layer of  $\text{SiO}_2$  of the  
19 same thickness but grown on single crystal silicon, rather  
20 than on polycrystalline silicon. Another problem present  
21 when using the sandwich formed by poly floating gate 15,  
22  $\text{SiO}_2$  dielectric 18 and poly control gate 16 is caused by  
23 the growth of polysilicon grains after oxide formation.  
24 These grains are often large enough to punch through the  
25 thin dielectric layer 18 (see Figure 3), thereby causing  
26 an electrical short between control gate 16 and floating  
27 gate 15 (Figure 1a). Silicon grains which do not punch  
28 through the dielectric layer 18 reduce the thickness of  
29 layer 18, and thus reduce the dielectric strength of  
30 dielectric layer 18.

31

32 One possible way to achieve high capacitance between  
33 control gate 16 and floating gate 15 is to form dielectric  
34 18 from materials with dielectric constants greater than  
35 the dielectric constant of  $\text{SiO}_2$ , such as tantalum oxide  
36 or other oxides so that, for a given capacitance, the  
37 dielectric layer 18 made from these materials does not  
38

1 need to be as thin as a dielectric layer 18 formed of  
2  $\text{SiO}_2$ . However, these materials do not have insulation  
3 properties as good as silicon dioxide due to poor material  
4 composition control and structural instability at high  
5 temperatures. Furthermore, the formation of such other  
6 oxides are not compatible with current integrated circuit  
7 processes and thus such other oxides cannot be easily  
8 implemented in nonvolatile integrated circuit memories.  
9

10 The use of a composite layer of silicon-rich  $\text{SiO}_2$ /  
11  $\text{SiO}_2$ /silicon-rich  $\text{SiO}_2$  between the floating gate and the  
12 control gate of a memory device has been described by D.J.  
13 Dimaria et al. in an article entitled, "High Current  
14 Injection Into  $\text{SiO}_2$  Using Si-rich  $\text{SiO}_2$  Films and Experimental  
15 Applications", The Physics of MOS Insulators, G. Lucovsky,  
16 et al. Ed. 1980. The structure described by Dimaria is  
17 shown in Figure 4a. Dielectric layer 44 is formed between  
18 polysilicon control gate 46 and polysilicon floating gate  
19 45. Dielectric layer 44 includes three layers 44a, 44b and  
20 44c as shown in more detail in Figure 4b. Layers 44a and  
21 44c are formed of silicon-rich silicon dioxide (i.e.  
22 silicon dioxide including an abundance of excess silicon  
23 atoms), and layer 44b is formed of substantially pure  
24 silicon dioxide. The operation of the Dimaria EEPROM  
25 shown in Figure 4 is similar to the prior art EEPROM shown  
26 in Figure 1a with one significant difference: floating  
27 gate 45 is charged and discharged through control gate 46,  
28 and three layer structure 44 is used to inject tunnelling  
29 electrons between control gate 46 and floating gate 45  
30 through dielectric 44 to either charge or discharge floating  
31 gate 45, as desired. When floating gate 45 is charged  
32 positive by causing electrons to tunnel out of the floating  
33 gate 45 through dielectric layer 44 into control gate 46,  
34 the control gate threshold voltage of Dimaria's transistor  
35 140 is decreased, thus storing a logical one. Conversely,  
36 when floating gate 45 is discharged by causing electrons  
37 to tunnel from control gate 46 through dielectric 44 into  
38

1 floating gate 45, the control gate threshold voltage of  
2 Dimaria's transistor 140 is increased, thus storing a  
3 logical zero. As described by Dimaria, by forming a thin  
4  $\text{SiO}_2$  layer between two layers of silicon-rich  $\text{SiO}_2$ , the  
5 current injection through the center  $\text{SiO}_2$  layer is consider-  
6 ably enhanced as compared with the current injection  
7 through a single layer of  $\text{SiO}_2$  having a thickness equal to  
8 the center  $\text{SiO}_2$  layer of the dielectric sandwich. Accord-  
9 ingly, this three layer dielectric structure is sometimes  
10 referred to as a "Dual Electron Injector Structure" (DEIS).

11

12 SUMMARY

13

14 In accordance with the teachings of this invention, a  
15 unique EEPROM device and a unique EPROM device are provided  
16 with a composite dielectric layer between the control gate  
17 and the floating gate which is sufficiently thick to  
18 provide electrical and physical integrity but also has a  
19 high equivalent dielectric constant. The composite dielec-  
20 tric layer is fabricated using methods which are compatible  
21 with the methods used to fabricate integrated circuits in  
22 a silicon substrate. The use of the composite dielectric  
23 layer in accordance with the teachings of this invention  
24 alleviates certain problems experienced in the prior art  
25 EPROM and EEPROM devices which utilize a polycrystalline  
26 silicon floating gate and a polycrystalline silicon control  
27 gate separated by an  $\text{SiO}_2$  dielectric layer, such as the  
28 problems of sharp silicon points causing low dielectric  
29 breakdown strength and the puncturing of the dielectric  
30 layer by polysilicon grain growth. In accordance with the  
31 teachings of this invention, a memory device includes  
32 buffering layers (i.e. layers which buffers abnormally  
33 high electric fields at sharp points and prevents poly-  
34 silicon grain growth from punching through the thin  
35 dielectric oxide) of silicon-rich  $\text{SiO}_2$  between the poly-  
36 silicon control gate and the silicon dioxide, and between  
37 the polysilicon floating gate and the silicon dioxide.

38

1 In contrast to the prior art use of a composite  
2 dielectric layer as an electron injection structure (equi-  
3 valent to a tunnel oxide) between the floating gate and  
4 the control gate of an EEPROM device, in accordance with  
5 one embodiment of this invention, a composite dielectric  
6 layer serves as a partially relaxable dielectric between  
7 the control gate and the floating gate of an EEPROM or an  
8 EPROM. The composite dielectric layer provides high  
9 capacitance between the floating gate and the control gate  
10 without the insulative and breakdown problems encountered  
11 with prior art thin dielectric layers, with electron  
12 injection taking place through the gate oxide between the  
13 drain extension and the floating gate, (EEPROM), and  
14 between the channel and the floating gate (EPROM).  
15

16 In another embodiment of this invention, the composite  
17 dielectric layer is implemented between the drain extension  
18 (EEPROM) or the channel (EPROM) and the floating gate and  
19 serves as the tunnel oxide, thereby providing increased  
20 tunnelling efficiency as compared to prior art structures  
21 which utilize a single layer of tunnelling oxide. The  
22 invention will be further understood with reference to the  
23 detailed description taken together with the drawings.  
24

#### 25 BRIEF DESCRIPTION OF THE DRAWINGS

26  
27 Figure 1a is a cross-sectional view of a typical  
28 prior art EEPROM;  
29

30 Figure 1b is a cross-sectional view of a typical  
31 prior art EPROM;  
32

33 Figure 2 depicts the mechanism of charge leakage and  
34 formation of local high electric fields due to asperities  
35 along polysilicon/SiO<sub>2</sub> interfaces;  
36  
37  
38

1        Figure 3 depicts the growth of silicon grains in a  
2        SiO<sub>2</sub> region formed adjacent to a polysilicon layer;

3  
4        Figure 4a is a cross-sectional view of a prior art  
5        EEPROM incorporating a Dual Electron Injector Structure  
6        (DEIS);

7  
8        Figure 4b is a detailed cross-sectional view of the  
9        DEIS structure of Figure 4a;

10  
11       Figure 5a is a cross-sectional view of two electrical  
12       conductors separated by a partially relaxable composite  
13       dielectric structure;

14  
15       Figure 5b depicts the charge transfer which occurs  
16       when a voltage is applied to the structure of Figure 5a;

17  
18       Figures 5c-5e are graphical representations of the  
19       qualitative behavior of the structure of Figure 5a;

20  
21       Figure 6 is a cross-sectional view of an EEPROM  
22       constructed in accordance with one embodiment of this  
23       invention utilizing a composite dielectric layer between  
24       the control gate and the floating gate and a tunnel oxide  
25       between the floating gate and the drain;

26  
27       Figure 7 is a cross-sectional view of an EPROM con-  
28       structed in accordance with another embodiment of this  
29       invention;

30  
31       Figures 8a and 8b are a plan view and a cross-sectional  
32       view, respectively, of a two-transistor EEPROM cell con-  
33       structed in accordance with one embodiment of this invention;  
34       and

35  
36       Figures 9-17 are cross-sectional views depicting one  
37       process for fabricating the structure of Figures 8a and  
38       8b.

1 DETAILED DESCRIPTION

2  
3 Figure 6 shows one embodiment of an EEPROM cell 78  
4 constructed in accordance with this invention. EEPROM  
5 cell 78 is formed in P type silicon 79, and includes N  
6 type source 83, N type drain 84, field oxide 87, gate  
7 oxide 87a, floating gate 81, control gate 80, and  
8 partially relaxable composite dielectric 86. EEPROM cell  
9 78 also includes tunnel oxide 85 located between N type  
10 drain region 84 and floating gate 81. Tunnel oxide 85  
11 allows tunnelling of electrons between floating gate 81  
12 and N type drain region 84 in order to program and erase  
13 cell 78, as previously described in conjunction with prior  
14 art EEPROMs.  
15

16 Composite dielectric layer 86 formed between control  
17 gate 80 and floating gate 81 is shown in more detail in  
18 Figure 5a. Composite dielectric layer 86 is formed of  
19 silicon-rich  $\text{SiO}_2$  layer 86a,  $\text{SiO}_2$  layer 86b and silicon-  
20 rich  $\text{SiO}_2$  layer 86c. The top and bottom layers 86a and  
21 86c of partially relaxable dielectric 86 are so-called  
22 "silicon-rich"  $\text{SiO}_2$  layers, meaning that layers 86a and  
23 86c have an abundance of free silicon atoms. Although  
24 silicon-rich  $\text{SiO}_2$  layers 86a and 86c are not used for  
25 electron injection, as taught by DiMaria, when  $\text{SiO}_2$  layers  
26 86a and 86c are used as a partially relaxable dielectric  
27 in accordance with this invention, silicon-rich  $\text{SiO}_2$   
28 layers 86a and 86c are preferably formed with a free  
29 silicon content in the range of 40 to 65 atomic percent,  
30 similar to the free silicon content used by DeMaria, et  
31 al. The thickness of the silicon-rich  $\text{SiO}_2$  layers 86a and  
32 86b is preferably between approximately 150Å to 500Å,  
33 because thicker layers have longer relaxation times (more  
34 fully described later) and thinner layers reduce the  
35 physical integrity of the composite dielectric layer 86,  
36 thus increasing the possibility of a short circuit between  
37 control gate 80 and floating gate 81 through composite  
38

1 dielectric layer 86. The center layer 86b of composite  
2 dielectric layer 86 is a layer of silicon dioxide, prefer-  
3 ably having a thickness within the range of approximately  
4 100Å to 300Å. Thicker intermediate layers 86b of  $\text{SiO}_2$   
5 provide decreased capacitance between control gate 80 and  
6 floating gate 81 and thinner layers provide a low dielec-  
7 tric breakdown strength of composite dielectric layer 86.

8  
9 Layers 86a and 86c of silicon-rich  $\text{SiO}_2$  are referred  
10 to as "relaxable" in that, when an electric field is  
11 applied between the control gate 81 and floating gate 82,  
12 layers 86a and 86c have sufficient conductivity to allow  
13 charges from control gate 81 and floating gate 81 to be  
14 transported to the upper and lower surfaces, respectively,  
15 of layer 86c and 86a in a short period of time (the  
16 "relaxation time"), as shown in Figure 5b, after which any  
17 further increase in the magnitude of the electric field  
18 will further increase the charge across the dielectric  
19 layer 86b, and relaxable dielectric layers 86a and 86c  
20 behave electrically as part of control gate 80 and floating  
21 gate 81, respectively. Dimaria teaches that a similar  
22 sandwich structure is utilized to inject electrons into  
23 the floating gate, not as a partially relaxable dielectric  
24 to increase capacitive coupling. In contrast to the  
25 structure of Dimaria, electrons do not tunnel from control  
26 gate 80 to floating gate 81 through dielectric 86 of the  
27 present invention because in this invention only a small  
28 fraction of the high applied voltage appears across the  
29 coupling dielectric 86. This is because the "coupling  
30 ratio" (described in more detail later) of the structure  
31 78 is very different from Dimaria's cell 140.

32  
33 The relaxation time T is defined as the time required  
34 after the initial application of a voltage  $V_0$  across  
35 control gate 80 and floating gate 81 until relaxable  
36 dielectric layers 86a and 86c behave electrically as part  
37 of the control gate 80 and floating gate 81, respectively.  
38

1 Relaxable dielectric layers 86a and 86c are considered to  
2 behave electrically as part of control gate 80 and floating  
3 gate 81, respectively, when the voltage across dielectric  
4 layer 86b is equal to approximately 95% of the voltage  
5 between control gate 80 and floating gate 81. The relaxation  
6 time T is inversely proportional to the conductivity of  
7 relaxable dielectric layers 86a and 86c. Also, the conduc-  
8 tivity of the layers 86a and 86c increases exponentially  
9 with the electric field across layers 86a and 86c, respec-  
10 tively. Preferably the relaxation time T is made very  
11 short by choosing suitable conductivities of relaxable  
12 dielectric layers 86a and 86c as determined by the propor-  
13 tion of free silicon atoms within the relaxable dielectric  
14 layers 86a, 86c. For example, for a relaxation time T on  
15 the order of 10 to 100 microseconds, the required conduc-  
16 tivities of relaxable dielectric layers 86a and 86c is met  
17 by having a free silicon content of layers 86a and 86c of  
18 approximately 40-65%. When relaxation of layers 86a and  
19 86c has occurred, there is a small sustaining electric  
20 field in layers 86a and 86c which support the space charges  
21 within the layers 86a and 86c. This sustaining electric  
22 field is very small (i.e. much less than  $10^6$  volts/cm if  
23 layers 86a and 86c have a sufficiently high conductivity,  
24 corresponding to a free silicon content of layers 86a and  
25 86c of approximately 50 atomic percent).

26  
27 Figures 5c, 5d and 5e depict in graphical form the  
28 qualitative behavior of the partially relaxable composite  
29 dielectric layer 86 of Figure 5a. After the application  
30 of an electric field to dielectric 86 and before relaxation  
31 time T has elapsed, layers 86a and 86c are not yet fully  
32 relaxed and behave electrically as part of the total  
33 dielectric composite layer 86, rather than as part of  
34 control gate 80 and floating gate 81, respectively. After  
35 relaxation time T has lapsed, layers 86a and 86c are fully  
36 relaxed and behave electrically as part of control gate 80  
37 and floating gate 81, respectively, and the dielectric  
38

1 breakdown voltage of the composite dielectric layer 86 is  
2 equal to the breakdown voltage of dielectric layer 86b.  
3 Figure 5c shows the voltage  $V_0$  applied across the composite  
4 dielectric layer 86b of Figure 5a. Figure 5d shows the  
5 change in voltage across the center dielectric layer 86b  
6 with respect to time and Figure 5e shows the change in  
7 capacitance between control gate 80 and floating gate 81  
8 as a function of time after the application at time  $t=0$  of  
9 a voltage  $V_0$  between control gate 80 and floating gate 81.  
10 If the relaxation time  $T$  and the sustaining voltage  $V_{sus}$   
11 (the voltage required to maintain the space charge across  
12 layers 86a and 86c) are both small (i.e.  $T \ll 10$  milliseconds,  
13  $V_{sus} \ll 10$  volts), the composite dielectric structure 86 is  
14 capacitively equivalent (when  $t > T$ ) to the use of a single  
15 layer 86b, even though the total thickness is that of all  
16 three layers 86a, 86b and 86c.

17  
18 In typical prior art EEPROM devices, the write and  
19 erase operations are performed by applying an approximately  
20 20 volt pulse of approximately 10 millisecond duration to  
21 control gate 16 of EEPROM 19 of Figure 1a. In accordance  
22 with this invention, the write and erase operations are  
23 performed with the composite dielectric layer 86 of Figures  
24 5a and 6 used in place of the 600-700Å layer 18 of  $\text{SiO}_2$   
25 (Figure 1) used in prior art EEPROMS. Since excellent  
26 physical and electrical integrity is achieved with the  
27 composite dielectric structure of Fig. 5a, the center  $\text{SiO}_2$   
28 layer 86b can be as thin as only 100Å without losing  
29 dielectric integrity. Capacitive coupling between control  
30 gate 80 and floating gate 81 of an EEPROM constructed in  
31 accordance with the principles of this invention is enhanced  
32 by 6 to 7 times as compared to prior art EEPROM structures  
33 which utilize a 600-700Å layer of  $\text{SiO}_2$  as the dielectric  
34 between the control gate and the floating gate.

35  
36 The silicon-rich  $\text{SiO}_2$  layer is a two-phase mixture of  
37 silicon and  $\text{SiO}_2$ , in that very small silicon particles are  
38

1 dispersed throughout the silicon-rich  $\text{SiO}_2$  layer. This  
2 silicon-rich  $\text{SiO}_2$  layer is very stable at the high temper-  
3 atures (typically approximately  $1100^\circ\text{C}$ ) often encountered  
4 in semiconductor processing. Furthermore, the silicon  
5 particles or "grains" formed within the silicon-rich  $\text{SiO}_2$   
6 layer rapidly reach a saturated size (do not grow further)  
7 of about  $100\text{\AA}$  because of a limited amount of excess silicon  
8 in the oxide, thus limiting silicon grain size to approximate  
9  $100\text{\AA}$ . This is in stark contrast to prior art memory  
10 structures where large silicon grains may penetrate into  
11 the  $\text{SiO}_2$  layer formed adjacent to polysilicon layers.  
12 There is no conglomeration of silicon grains upon further  
13 processing of the semiconductor device because silicon  
14 atoms have very small diffusivities in oxide, thus prevent-  
15 ing the formation of larger silicon grains within the  
16 silicon-rich  $\text{SiO}_2$  layers 86a and 86c or the  $\text{SiO}_2$  layer 86b  
17 (Figure 5a). Because of the chemical stability of the  
18 composite dielectric layer 86, a considerable yield improve-  
19 ment is achieved as compared with the yield of prior art  
20 devices utilizing only a single  $\text{SiO}_2$  dielectric layer  
21 between the polysilicon control gate 16 and floating gate  
22 15 (Figure 1).  
23

24 In accordance with the present invention, the capaci-  
25 tance  $C_1$  between control gate 80 and floating gate 81  
26 (Figure 6) is enhanced by as much as 6 to 7 times over  
27 prior art structures using a single  $\text{SiO}_2$  dielectric layer  
28 between the control gate and the floating gate. If the  
29 capacitance between the floating gate 81 and the drain 84  
30 is  $C_2$ , then the coupling ratio  $\eta$  of control gate 80 to  
31 floating gate 81, is defined (neglecting parasitic capaci-  
32 tances) as:  
33

$$34 \quad \eta = C_1 / (C_1 + C_2)$$

35  
36 where  $\eta$  = control gate 80 to floating gate 81  
37 coupling ratio;  
38

1            $C_1$  = capacitance between control gate 80  
2                      and floating gate 81;  
3            $C_2$  = capacitance between floating gate 81  
4                      and drain 84.  
5

6           For a given capacitance  $C_2$  (mostly due to the capaci-  
7           tance provided due to tunnel oxide 85 serving as the  
8           dielectric between floating gate 81 and drain 84), an  
9           increased capacitance  $C_1$  provides an increased coupling  
10          ratio  $\eta$  and hence a lower programming voltage is required  
11          to be applied to control gate 80 in order to capacitively  
12          couple a given voltage to floating gate 81 to program the  
13          cell 78. Alternatively, for a given capacitance  $C_2$ , an  
14          increased capacitance  $C_1$  reduces the floating gate 81 area  
15          (when viewed from the top of the cell 78) required to  
16          achieve a given coupling ratio  $\eta$  necessary to allow pro-  
17          gramming of cell 78 with a given programming voltage  
18          applied to control gate 80. This decreased size of floating  
19          gate 80 reduces the size of cell 78, thus allowing the  
20          fabrication of a memory array comprising a plurality of  
21          cells 78 which is more dense than the memory arrays of the  
22          prior art.  
23

24          Referring again to Figure 5a, the three layer composite  
25          dielectric is made, for example, by low pressure chemical  
26          vapor deposition (CVD) techniques well known in the semi-  
27          conductor industry. For example, by adjusting the gas  
28          flow rate ratio of two active gases  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  at a CVD  
29          reaction temperature of  $700^\circ\text{C}$ , layers of silicon-rich  $\text{SiO}_2$   
30          and pure  $\text{SiO}_2$  are deposited sequentially. Other methods  
31          are also available to fabricate the partially relaxable  
32          dielectric 86, for example LPCVD (Low Pressure CVD), which  
33          is the use of LPCVD is believed to be the better fabrication  
34          method for volume production because of typically better  
35          film uniformity. Such LPCVD techniques are described, for  
36          example in the article by Rosler entitled "Low Pressure  
37          CVD Production Process for Poly, Nitride, and Oxide",  
38          Solid State Technology, April 1977, pages 63-70.

1       The silicon-rich  $\text{SiO}_2/\text{SiO}_2/\text{silicon-rich SiO}_2$  structure  
2 is only one composite dielectric which is suitable for use  
3 in accordance with the teachings of this invention. Other  
4 embodiments of this invention utilize silicon-rich  $\text{Si}_3\text{N}_4$   
5 as a relaxable dielectric. Such embodiments of this  
6 invention form a composite dielectric layer of silicon-rich  
7  $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{silicon-rich Si}_3\text{N}_4$  or silicon-rich  $\text{Si}_3\text{N}_4/\text{Si}_3\text{N}_4/\text{silicon-rich Si}_3\text{N}_4$ .  
8 Methods for fabricating such composite  
9 dielectric structures are obvious to one of ordinary skill  
10 in the art in light of the teachings of this specification.  
11 For example, CVD processes utilizing  $\text{SiH}_4$  and  $\text{N}_2$  gases  
12 can be used for  $\text{Si}_3\text{N}_4$  and Si-rich  $\text{Si}_3\text{N}_4$ .  
13

14       Tunnel oxide 85 in one embodiment of the EEPROM of  
15 Figure 6 is thermal oxide of approximately  $100\text{\AA}$  in thickness.  
16 In another embodiment, tunnel oxide 85 is a silicon-rich  
17  $\text{SiO}_2/\text{SiO}_2/\text{silicon-rich SiO}_2$  composite dielectric layer  
18 similar to the composite dielectric 86, thus providing  
19 enhanced current injection between drain 84 and floating  
20 gate 81 as compared to prior art EEPROMs utilizing a  
21 single  $\text{SiO}_2$  layer as tunnel oxide 85, thereby allowing the  
22 use of a lower write/erase voltage for programming the  
23 cell 78. In this embodiment of my invention, two separate  
24 partially relaxable dielectric layers serve two purposes:  
25 enhancement of the capacitance between the control gate 80  
26 and floating gate 81, and enhancement of the tunnel current  
27 between floating gate 81 and drain 84 during programming  
28 and erasure of cell 78. In contrast to DiMaria, electron  
29 tunnelling between control gate 80 and floating gate 81 is  
30 avoided by the fact that the majority of the write/erase  
31 voltage (e.g. 70%) appears across the tunnel oxide 85, and  
32 only a small fraction (e.g. 30%) of the voltage appears  
33 across the partially relaxable composite dielectric 86.  
34

35       One embodiment of an EPROM constructed in accordance  
36 with the teachings of the present invention is shown in  
37 the cross-sectional view of Figure 7. In an EPROM con-  
38

1 structured in accordance with the principles of this invention,  
2 partially relaxable dielectric layer 96 formed between  
3 polysilicon control gate 90 and polysilicon floating gate  
4 91 greatly enhances capacitive coupling between control  
5 gate 90 and floating gate 91, and therefore a lower pro-  
6 gramming voltage on the control gate 90 can be used, as  
7 compared with prior art EPROM devices. Since an EPROM  
8 constructed in accordance with this invention can achieve  
9 a given capacitance value  $C_1$  between floating gate 91 and  
10 control gate 90 with much less floating gate area as  
11 compared to prior art EPROM cells, a smaller EPROM cell is  
12 achieved for a given programming voltage, thereby allowing  
13 the formation of more dense arrays of memory cells.

14  
15 Figures 8a and 8b show one embodiment of a two-  
16 transistor EEPROM cell 200 constructed in accordance with  
17 the teachings of this invention. Figure 8a is a top view  
18 of cell 200 and Figure 8b is a cross-sectional view drawn  
19 along the line AA of Figure 8a. P type substrate 307, N  
20 type source region 106, N type drain 104, word line 103,  
21 electrical contact 107, and transistor channel 110 form a  
22 MOSFET 201 used as a "select" transistor 201. The select  
23 transistor 201 is used to provide the selective writing,  
24 erasing and reading of cell 200, in a manner which is well  
25 known in the prior art. The left sides of Figures 8a and  
26 8b show the memory MOSFET 202, having a floating gate 101  
27 capable of storing a charge representing the data stored  
28 in cell 200. Partially relaxable dielectric 102, comprising  
29 a sandwich of silicon-rich  $\text{SiO}_2/\text{SiO}_2/\text{silicon-rich SiO}_2$ , is  
30 incorporated between floating gate 101 and control gate  
31 100.

32  
33 To program the cell 200 to a logical one, high voltages  
34 (typically 15 volts) are selectively applied to both word  
35 line 103 and metal bit line 109 which makes contact with  
36 drain 104 of the select transistor 201. The high voltage  
37 on drain 104 is transferred through channel 110 to N type  
38

1 region 106. Control gate 100 is connected to ground.  
2 Partially relaxable composite dielectric 102 provides high  
3 capacitive coupling between the polysilicon control gate  
4 100 and polysilicon floating gate 101. Therefore, floating  
5 gate 101 is capacitively coupled to ground. Tunnel oxide  
6 105 between N type region 106 (high voltage) and floating  
7 gate 101 (near ground) allow electrons to tunnel out of  
8 floating gate 101 through tunneling dielectric 105 into N  
9 type region 106, thereby programming the memory transistor  
10 202 with a positive charge on floating gate 101. After  
11 programming of memory transistor 202, the positive charge  
12 is retained on floating gate 101 (unless erased) for an  
13 extremely long period of time, typically ten years. The  
14 positive charge stored on floating gate 101 decreases the  
15 control gate threshold voltage of memory transistor 202.  
16 This decreased threshold voltage denotes a logical zero.  
17

18 To erase the memory transistor 202, drain 104 is  
19 connected to ground, and a high voltage is applied to word  
20 line 103 and control gate 100; floating gate 101 is capaci-  
21 tively coupled to the high voltage on control gate 100.  
22 The low drain 104 voltage is applied through channel 110  
23 to N type region 106 and erasing occurs as electrons are  
24 injected from N type region 106, through tunnel dielectric  
25 105, into floating gate 101. Thus, floating gate 101  
26 becomes negatively charged, raising the control gate  
27 threshold voltage of memory transistor 202. This high  
28 threshold voltage denotes a logical one.  
29

30 One process for fabricating devices in accordance  
31 with this invention will be described with reference to  
32 Figures 9-17. Silicon substrate 109 is covered by a base  
33 layer of silicon dioxide 120 having a thickness of 400-1000  
34 angstroms. Hereinafter, the entire structure at various  
35 stages in the fabrication process will be referred to as a  
36 "wafer". Base oxide 120 is formed, for example, by oxidiz-  
37 ing the wafer in a wet oxygen atmosphere at approximately  
38

1 920°C for approximately 15-30 minutes. A layer of nitride  
2 (not shown) is then deposited on top of the base oxide 120  
3 to a thickness of 400-1500Å, for example, by conventional  
4 chemical vapor deposition. Well known photolithographic  
5 and etching techniques are then used to pattern the  
6 nitride layer to define areas in which active devices are  
7 to be formed. Channel stops 122 are then formed, for  
8 example by the ion implantation of boron at approximately  
9 80 KEV to a dosage of approximately  $10^{13}$  atoms/cm<sup>2</sup>. Field  
10 oxide 121 is grown to a thickness of approximately 1  
11 micron, for example, by oxidation in wet oxygen at approxi-  
12 mately 900°C for approximately 20 hours. The remaining  
13 portions of the masking nitride is then removed, for  
14 example by etching with phosphoric acid, providing the  
15 structure shown in Figure 9.

16  
17 Referring to Figure 10 (field oxide 121 is not shown  
18 in Figs. 10-17 for simplicity), a photoresist pattern 125  
19 is used in a well known manner to define transistor channels  
20 110 and 111, and the exposed portions of base oxide 120  
21 are removed, for example by etching with buffered HF. The  
22 exposed surface of the wafer is then doped to form heavily  
23 doped N regions 104, 106 and 108, for example by ion  
24 implantation of arsenic at approximately 100 KEV to a  
25 dosage of approximately  $10^{16}$  atoms/cm<sup>2</sup>.

26  
27 Referring to Figure 11, photoresist 125 is removed,  
28 followed by the sequential formation of three layers:  
29 150Å silicon-rich SiO<sub>2</sub> layer 128, 100Å SiO<sub>2</sub> layer 129, and  
30 150Å silicon-rich SiO<sub>2</sub> layer 130, thereby forming composite  
31 dielectric layer 140. The atomic percent of silicon in  
32 silicon-rich SiO<sub>2</sub> layers 128 and 130 is typically in the  
33 range of 40% to 65%. In one embodiment, the deposition  
34 process utilizes chemical vapor deposition (CVD) methods.  
35 By properly adjusting the ratio of the reacting gases,  
36 SiH<sub>4</sub> and N<sub>2</sub>O, at a deposition temperature of 700°C, all  
37 three layers are deposited in one CVD run. For instance,  
38

1 a  $\text{SiF}_4/\text{N}_2\text{O}$  ratio within the range of 3:1 to 10:1 can be  
2 used. Another method of forming the composite dielectric  
3 layer 140 is Low Pressure CVD, which gives better uniformity  
4 and higher throughput.  
5

6 After deposition of composite dielectric layer 140, a  
7 layer 133 (Figure 12) of approximately 1000Å undoped poly-  
8 silicon is formed, for example by low pressure CVD. A  
9 layer 134 of approximately 500Å silicon nitride ( $\text{Si}_3\text{N}_4$ ) is  
10 then formed, for example by low pressure CVD. Polysilicon  
11 layer 133 is preferably deposited by the decomposition of  
12  $\text{SiF}_4$  gas in the same CVD reactor as is used to form com-  
13 posite dielectric layer 140. Polysilicon layer 133 serves  
14 as a buffer layer between nitride layer 134 and underlying  
15 silicon-rich  $\text{SiO}_2$  layer 130. This buffer layer 133 protects  
16 Si-rich  $\text{SiO}_2$  layer 144 from contamination and chemical  
17 attack during later etching of masking nitride layer 134.  
18 Top nitride layer 134 is used to define tunnel dielectric  
19 140 in a novel "self-aligned" fashion, as described below.  
20 Transistor channel regions 110 and 111 are protected by  
21 base oxide 120 from contamination from silicon-rich  $\text{SiO}_2$   
22 layer 128 which otherwise is in direct contact with the  
23 surface of channels 110 and 111.  
24

25 Referring to Figure 12, photoresist layer 135 is  
26 formed and patterned in a well known manner to cover  
27 nitride layer 134 and undoped polysilicon layer 133 where  
28 tunnel dielectric 140 is to be formed. The exposed nitride  
29 and polysilicon layers are then removed, for example, by  
30 plasma etching using  $\text{CF}_4$  and  $\text{O}_2$  plasmas, respectively, at  
31 25°C. Remaining portions of photoresist 135 are then  
32 removed in a well known manner. The wafer is then thermally  
33 oxidized in wet or dry oxygen, thereby causing that portion  
34 of composite dielectric layer 140 which is exposed to be  
35 converted to pure  $\text{SiO}_2$ . The part of composite dielectric  
36 layer 140 which is protected by nitride layer 134 and  
37 polysilicon layer 133 is unaffected by this oxidation step  
38

1 because silicon nitride is oxidation resistant. Converted  
2 portions of composite dielectric layer 140 and the remaining  
3 base oxide 120 are then removed, for example by etching  
4 with a 10% HF solution at 23°C, leaving tunnel dielectric  
5 140 under nitride layer 134 and polysilicon layer 133  
6 (Figure 13).

7  
8 Referring now to Figure 14, with the remaining portion  
9 of nitride layer 134 protecting polysilicon layer 133 from  
10 oxidation, gate oxide layer 145 is formed on exposed  
11 portions of the surface of channels 110 and 111 to a  
12 thickness of approximately 400Å, for example by oxidation  
13 in wet O<sub>2</sub> at approximately 900°C for approximately 40  
14 minutes. Gate oxide 145 is also grown simultaneously over  
15 the heavily doped N regions 104, 106 and 108 and tends to  
16 be thicker (i.e. approximately 1000Å) than the gate oxide  
17 145 over the channel due to the increased oxidation rate  
18 of regions 104, 106 and 108 due to the presence of dopants  
19 therein. Nitride layer 134 is then removed, for example  
20 by etching with hot phosphoric acid at approximately 160°C  
21 for approximately 10 minutes. Gate oxide 145 and poly-  
22 silicon 133 have very low etch rates in phosphoric acid  
23 compared to nitride (i.e. approximately 20 Å/minute for  
24 nitride versus less than 1 Å/minute for oxide and poly),  
25 and thus are unaffected by the etching of nitride 134.

26  
27 Of importance, the use of nitride layer 134 and  
28 polysilicon 133 to define tunnel dielectric 140 has several  
29 advantages. For instance, there is no overlap of gate  
30 oxide 145 and tunnel dielectric 140; i.e, tunnel dielectric  
31 140 is "self-aligned" to gate oxide 145. Overlap regions  
32 not only waste cell area but also cause reliability problems  
33 due to charge trapping effects. A further advantage is  
34 that the silicon-rich SiO<sub>2</sub>/SiO<sub>2</sub>/silicon-rich SiO<sub>2</sub> composite  
35 tunnel dielectric 140 (Figures 11-14), which is made of  
36 ultra thin films (approximately 100-150Å thick) and is  
37 extremely sensitive to contamination and physical or  
38

1 chemical damage, is always protected during processing by  
2 a polysilicon buffer layer 133 (Figures 11-14). Further-  
3 more gate oxide layer 145 is formed independently of the  
4 formation of composite dielectric layer 140 and polysilicon  
5 layer 133, which provides gate oxide to layer 145 having  
6 much better quality as compared to gate oxide layers  
7 formed by other methods, for example, where undesired  
8 portions of composite dielectric layer 140 is removed from  
9 the top of gate oxide 120 (Figure 12) without using the  
10 above mentioned technique.  
11

12 Referring to Figure 15, polysilicon layer 150 is then  
13 formed to a thickness of approximately 3000Å, for example  
14 by CVD using  $\text{SiE}_4$  gas at approximately 620°C. Poly layer  
15 150 is then doped with, for example, phosphorus in a well  
16 known manner to reduce its resistivity to approximately  
17  $1 \times 10^{-3}$  ohm-cm. Partially relaxable composite dielectric  
18 structure 102 is then formed on doped polysilicon layer  
19 150. In one embodiment of this invention, composite  
20 dielectric structure 102 is formed of three layers con-  
21 sisting of 150Å silicon-rich  $\text{SiO}_2$ , 100Å  $\text{SiO}_2$  and 150Å  
22 silicon-rich  $\text{SiO}$ , although other thicknesses and materials  
23 can be used in accordance with the teachings of this  
24 invention. The silicon-rich  $\text{SiO}_2$  films are similar to  
25 those used to form composite tunnel dielectric 140. In one  
26 embodiment of this invention, more silicon atoms are  
27 incorporated into the silicon-rich  $\text{SiO}_2$  layers of composite  
28 dielectric 102 (e.g. 60% silicon) than the silicon-rich  
29  $\text{SiO}_2$  tunnelling dielectric 140 (e.g. 50% silicon), thus  
30 minimizing the relaxation time of dielectric layer 102 by  
31 increasing the conductivity of the silicon-rich  $\text{SiO}_2$   
32 layers within dielectric layer 102 due to their high  
33 silicon content.  
34

35 A 1000 Å undoped polysilicon layer 153 and a 500Å  
36 layer of silicon nitride 152 are formed on top of dielectric  
37 102 by, for example, LPCVD. A layer of photoresist (not  
38

1 shown) is formed and patterned in a well known manner to  
2 define floating gate 101. Unmasked portions of nitride  
3 layer 152 are removed, for example by etching with hot  
4 phosphoric acid. Unmasked portions of poly layer 153 and  
5 oxide 102 are then removed, for example by etching with  $O_2$   
6 plasma and buffered HF, respectively. A second photoresist  
7 layer 151 is then formed to define floating gate 101 and  
8 control gate 103. Unmasked portions of poly layer 150 are  
9 then removed, for example by plasma etching with  $O_2$  gas.  
10 Of importance, polysilicon layer 133 remaining on top of  
11 tunnel dielectric 140 is doped by and becomes part of  
12 polysilicon layer 150a, which in turn becomes floating  
13 gate 101. Portion 150b of polysilicon layer 150 forms  
14 word line 103.

15

16 Additional N type regions 156 are formed, for example  
17 by the ion implantation of arsenic at approximately 100  
18 KEV to a dosage of approximately  $10^{16}$  atoms/cm<sup>2</sup>, thereby  
19 connecting the gap between N type region 106 and word line  
20 103, and the gap between word line 103 and N type region  
21 104. Photoresist 151 is then removed in a well known  
22 manner.

23

24 Oxide 160 of (Figure 16) is then formed to a thickness  
25 of approximately 2000Å by, for example, thermal oxidation  
26 in wet oxygen at approximately 800°C, for approximately  
27 100 minutes. Nitride 152 is oxidation resistant and is  
28 not oxidized during the formation of sidewall oxide 160.  
29 Nitride 152 is then removed, for example by etching with  
30 hot phosphoric acid.

31

32 Polysilicon layer 175 (Figure 17) is then formed, for  
33 example by LPCVD and doped, for example with phosphorus to  
34 reduce its resistivity to approximately  $1 \times 10^{-3}$  ohm-cm.  
35 Photoresist 170 is formed and patterned in a well known  
36 manner to define the desired interconnect pattern of  
37 polysilicon layer 175, as shown in Figure 17. Exposed

38

1 portions of polysilicon 175 are then removed, for example  
2 by etching with  $CF_4$  plasma at 25°C and resist 170 is then  
3 removed in a well known manner. Oxidation of polysilicon  
4 layer 175 passivates layer 175 and also oxidizes exposed  
5 portions undoped polysilicon layer 153a. Unexposed poly-  
6 silicon layer 153b is doped by dopant diffusion from  
7 polysilicon layer 175 and, together with polysilicon layer  
8 175, forms control gate 100 of the structure shown in  
9 Figure 8b.

10  
11 Typical processing steps are then employed, for  
12 instance, doped glass deposition, contact doping, glass  
13 reflow and metal interconnect deposition and patterning.  
14 The completed structure is shown in Figure 8b. Either  
15 polysilicon layer 100 or polysilicon layer 101 is used as  
16 FET gates in periphery circuits, as desired. Conventional  
17 steps utilized in the fabrication of integrated circuit  
18 memory products, such as threshold adjustment implants,  
19 buried contacts, etc. are not described for brevity but  
20 are easily understood to those of ordinary skill in the  
21 art.

22  
23 While specific embodiments of this invention have been  
24 presented in the specification, these specific embodiments  
25 are intended to serve by way of example only and are not  
26 to be construed as limitations on the scope of this inven-  
27 tion. Numerous other embodiments of this invention will  
28 become readily apparent to those with ordinary skill in  
29 the art in light of the teachings of this specification.

1

CLAIMS

5

1. A Programmable Read Only Memory structure,  
comprising a plurality of cells each including :

10

a semi conductor substrate;  
a source (83, 93) formed within said substrate;  
a drain (84,94) formed within said substrate;  
a channel region formed within said substrate  
between said source and said drain;

15

a floating gate (81, 91) located above said  
channel and spaced apart from said channel by a gate  
dielectric (87a, 97); and

20

a control gate (80, 90) located above and  
separated from said floating gate (81, 91) by a dielectric  
(86, 96);

characterized in that at least one of said dielectrics  
is a partially relaxable dielectric wherein the charge  
stored on said floating gate is altered by the transfer of  
charge from said floating gate through said dielectric.

25

2. The structure as in Claim 1, characterized in  
that said partially relaxable dielectric comprises:

a first layer (86a) of a silicon-rich oxide of  
silicon;

a second layer (86c) of a silicon-rich oxide  
of silicon; and

30

a third layer (86b) of an oxide of silicon  
located between said first and said second layers.

35

3. The structure as in Claim 2, characterized in  
that said first and said second layers (86a, 86c) comprise  
approximately 40 to 65 % atomic percent silicon.

1           4. The structure as in Claim 2 or 3, characterized  
in that said first and said second layers (86a, 86c) each  
have thickness within the range of approximately 150Å to  
500Å.

5           5. The structure as in any one of Claims 2 to 4,  
characterized in that said third layer (86b) has a thickness  
within the range of approximately 100Å to 300Å.

10          6. The structure as in Claim 1, characterized in  
that said partially relaxable dielectric comprises:

          a first layer (86a) of silicon-rich silicon  
nitride;

          a second layer (86c) of silicon-rich silicon  
15 nitride; and

          a third layer (86b) of an oxide of silicon  
located between said first and said second layers.

20          7. The structure as in Claim 1, characterized in  
that said partially relaxable dielectric comprises:

          a first layer (86a) of silicon-rich silicon  
nitride;

          a second layer (86c) of silicon-rich silicon  
nitride; and

25           a third layer (86b) of silicon nitride located  
between said first and said second layers.

30          8. The structure as in any one of Claims 2 to 7,  
characterized in that said partially relaxable dielectric  
has a relaxation time within the range of approximately 10  
to 100 microseconds, where said relaxation time is defined  
as the time required between the application of a voltage  
across said first and second layers and the time when  
35 approximately 95 % of said voltage appears across said third  
layer.

1           9. The structure as in any one of Claims 1 to 8,  
characterized in that said gate dielectric includes a tunnel  
portion (85) having a thickness less than the thickness of  
the remainder of said gate dielectric, said tunnel portion  
5   (85) and said gate dielectric (86) comprising said partially  
relaxable dielectric.

          10. The structure of any one of Claims 1 to 8,  
characterized in that said charge on said floating gate (91)  
10 is removed by exposing said floating gate to ultraviolet  
light.

15

20

25

30

35

1/5

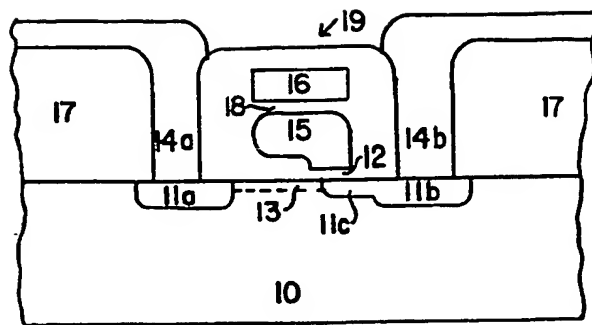


FIG. 1a

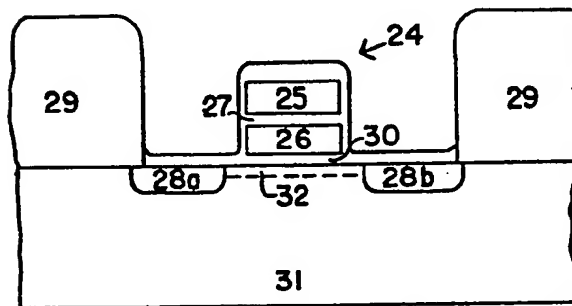


FIG. 1b

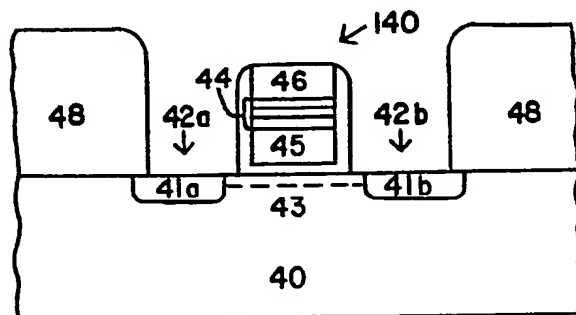


FIG. 4a

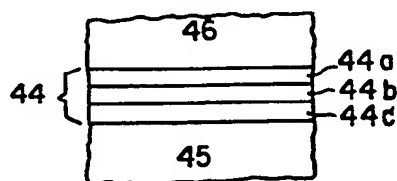


FIG. 4b

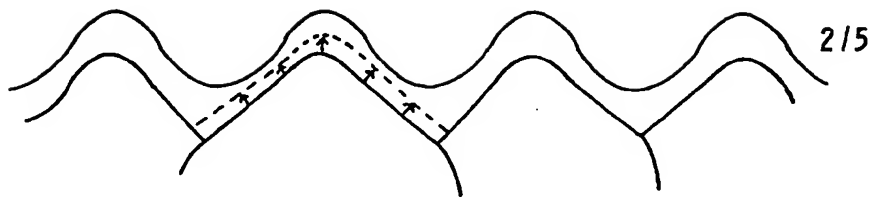


FIG. 3

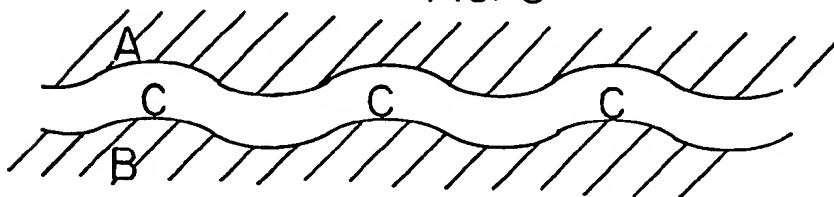


FIG. 2

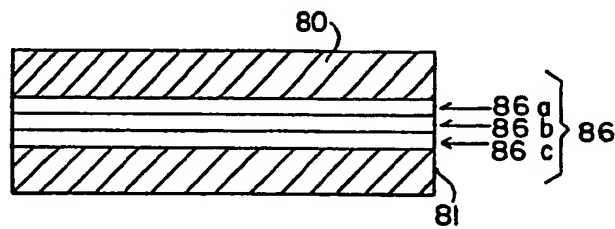


FIG. 5a

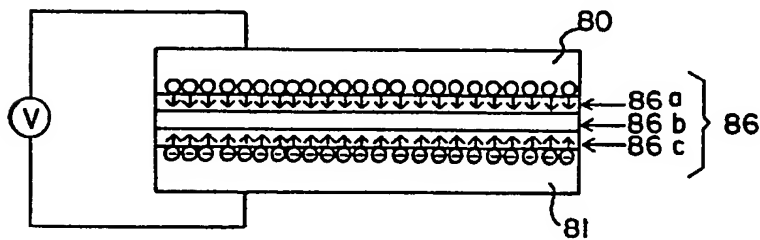


FIG. 5b

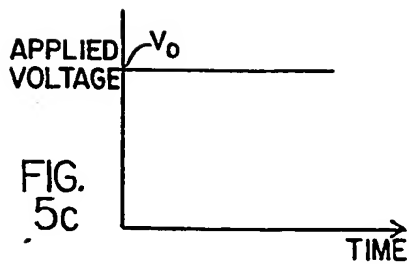


FIG. 5c

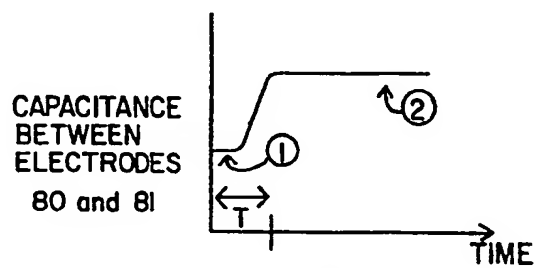


FIG. 5e

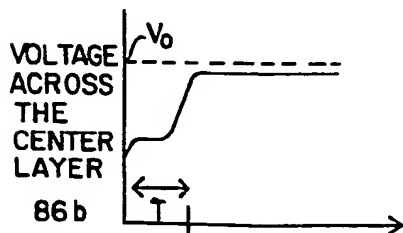


FIG. 5d

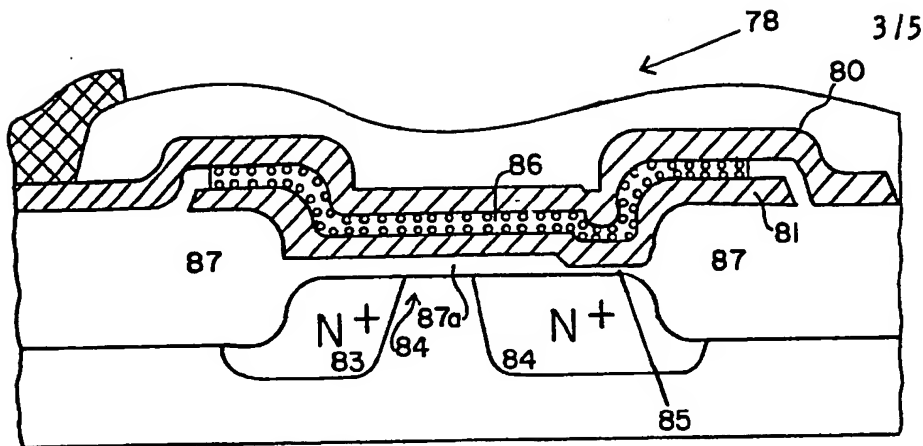


FIG. 6

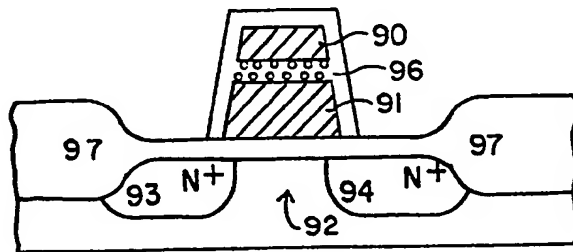


FIG. 7

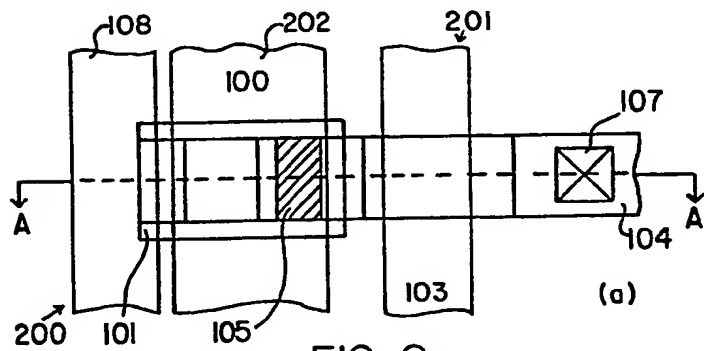


FIG. 8a

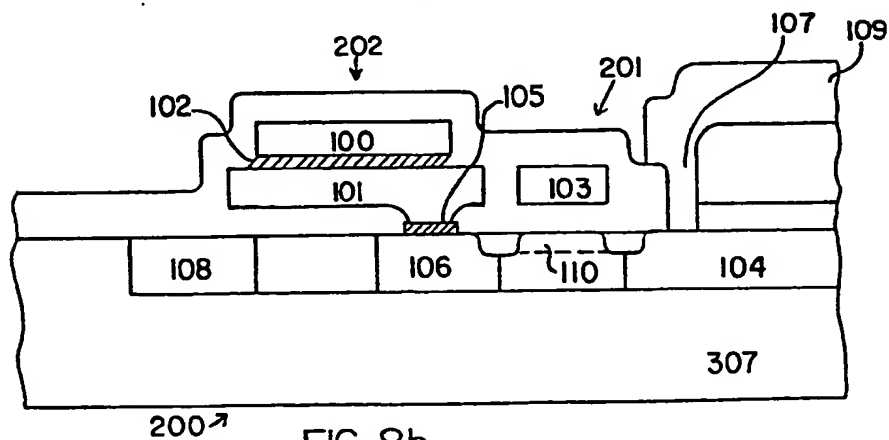


FIG. 8b

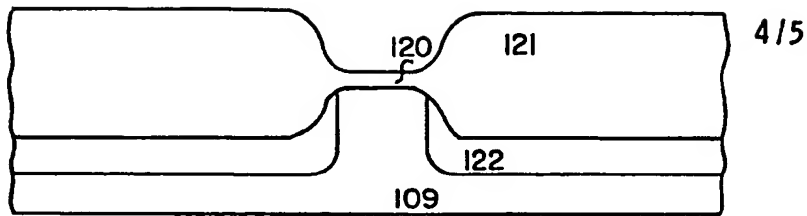


FIG. 9

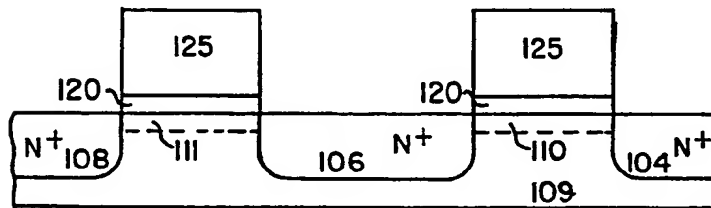


FIG. 10

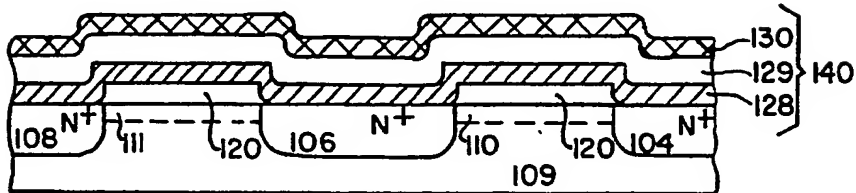


FIG. 11

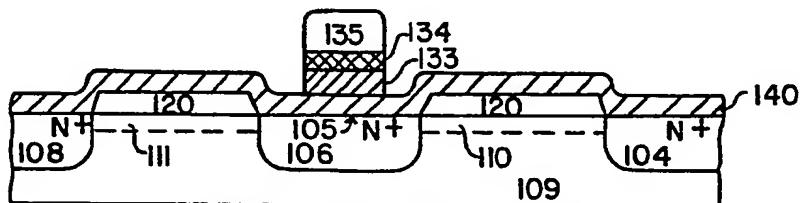


FIG. 12

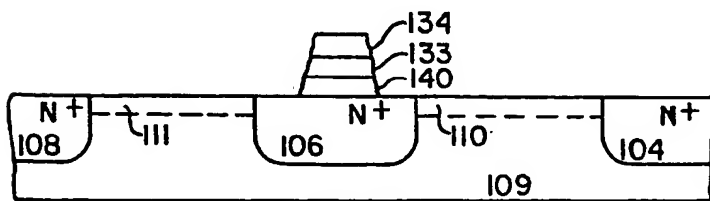


FIG. 13

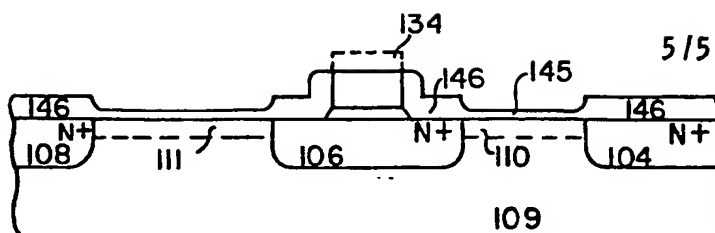
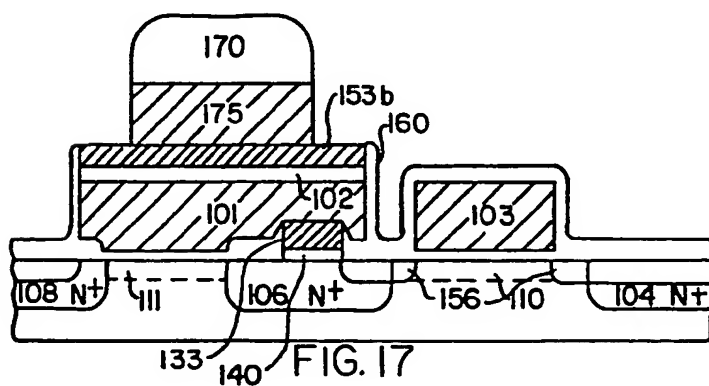
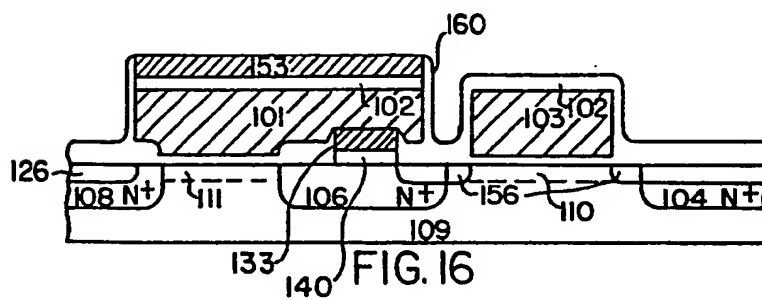
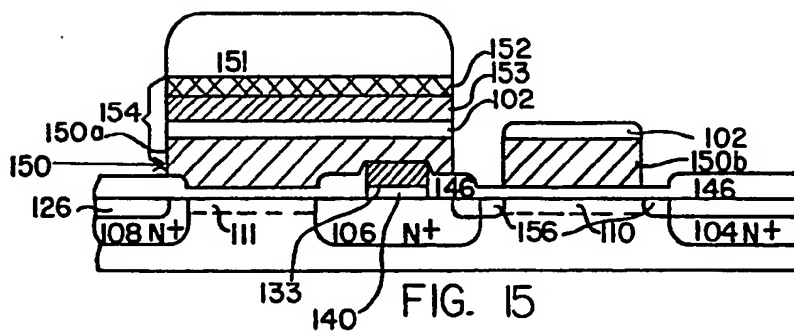


FIG. 14



17 **EUROPEAN PATENT APPLICATION**

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54 **Programmable read only memory.**

57 Unique EPROM and EEPROM devices are provided with a composite dielectric layer between the control gate and the floating gate which is sufficiently thick to provide electrical and physical integrity but also has a high equivalent dielectric constant. The use of the composite dielectric layer alleviates certain problems experienced in the prior art EPROM and EEPROM devices which utilize a polycrystalline silicon floating gate and a polycrystalline silicon control gate separated by an SiO<sub>2</sub> dielectric layer, such as the problems of sharp silicon points polysilicon grain growth causing low dielectric breakdown strength. In contrast to the prior art, a composite dielectric layer serves as a partially relaxable dielectric between the control gate and the floating gate of an EEPROM or an EPROM. The composite dielectric layer provides high capacitance between the floating gate and the control gate without the insulative and breakdown problems encountered with prior art thin dielectric layers, with electron injection taking place through the gate oxide between the drain extension and the floating gate, (EEPROM), and between the channel and the floating gate (EPROM). In another embodiment of this invention, the composite dielectric layer is implemented between the drain extension (EEPROM) or the channel (EPROM) and the floating gate and serves as the tunnel oxide.

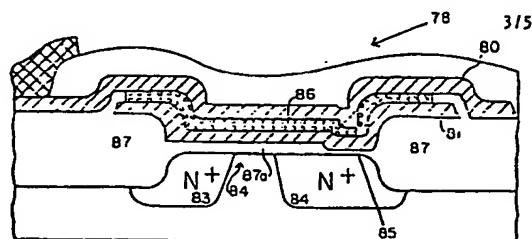


FIG. 6



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# EUROPEAN SEARCH REPORT

0105802  
Application number

EP 83 40 1908

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 7)
X	US-A-4 336 603 (IBM CORP.) * Figure 6; column 3, lines 48-55; column 7, lines 34-68; column 8, lines 1-21 *	1-3	H 01 L 29/60 G 11 C 27/00
X	--- EP-A-0 034 653 (IBM CORP.) * Figure 1; page 6, lines 1-25; page 13, lines 16-31 *	1-4, 6, 7	
A	--- IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, vol. 23, February 1980, pages 152-153, 271, IEEE, New York, US; W.S. JOHNSON et al.: "Session XII: ROMs, PROMs and EROMs. THPM 12.6: A 16Kb electrically erasable nonvolatile memory" * Whole article *	9, 10	
A	--- IEEE ELECTRON DEVICE LETTERS, vol. EDL-1, no. 9, September 1980, pages 179-181, IEEE, New York, US; D.J. DIMARIA et al.: "Electrically-alterable memory using a dual electron injector structure" * Whole document *	1-5	H 01 L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 14-11-1983	Examiner ALLEN E.F.
<b>CATEGORY OF CITED DOCUMENTS</b>			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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# EUROPEAN SEARCH REPORT

0105802

Application number

EP 83 40 1908

Page 2

DOCUMENTS CONSIDERED TO BE RELEVANT															
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)												
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-28, no. 9, September 1981, pages 1047-1053, IEEE, New York, US; D.J. DIMARIA et al.: "Dual-electron-injector-structure electrically alterable read-only-memory modeling studies" * Figure 1; page 1051 *	1-5													
A	EP-A-0 051 158 (IBM CORP.)														
P, X	EP-A-0 083 387 (IBM CORP.) * Figures 1,3; pages 6,8 *	1,2,9													
			TECHNICAL FIELDS SEARCHED (Int. Cl. 3)												
The present search report has been drawn up for all claims															
Place of search THE HAGUE		Date of completion of the search 14-11-1983	Examiner ALLEN E.F.												
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